**Сводный отчет использования ресурсов микросхемы Spartan6 при моделировании нейросети Элмана**

**Дискретная модель сети Элмана (4 входа, 8 нейронов, 9 бит/коэффициент)**

Primitive and Black Box Usage:

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# BELS : 2460

# GND : 1

# LUT2 : 66

# LUT3 : 406

# LUT4 : 583

# LUT5 : 8

# LUT6 : 27

# MUXCY : 640

# MUXF7 : 8

# VCC : 1

# XORCY : 720

# FlipFlops/Latches : 18

# FD : 2

# FDE : 16

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 442

# IBUF : 437

# OBUF : 5

Device utilization summary:

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Selected Device : 6slx16ftg256-3

Slice Logic Utilization:

Number of Slice Registers: 18

Number of Slice LUTs: 1090

Number used as Logic: 1090

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1098

Number with an unused Flip Flop: 1080

Number with an unused LUT: 8

Number of fully used LUT-FF pairs: 10

Number of unique control sets: 4

IO Utilization:

Number of IOs: 443

Number of bonded IOBs: 443

Minimum period: 11.667ns (Maximum Frequency: 85.714MHz)

Minimum input arrival time before clock: 12.237ns

Maximum output required time after clock: 22.268ns

Maximum combinational path delay: 22.839ns

**Непрерывная модель сети Элмана (4 входа, 8 нейронов, 32 бит/коэффициент)**

Primitive and Black Box Usage:

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# BELS : 9059

# GND : 1

# LUT2 : 274

# LUT3 : 1535

# LUT4 : 2072

# LUT5 : 4

# LUT6 : 76

# MUXCY : 2536

# VCC : 1

# XORCY : 2560

# FlipFlops/Latches : 11

# FD : 2

# FDE : 9

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 1546

# IBUF : 1541

# OBUF : 5

Device utilization summary:

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Selected Device : 6slx16ftg256-3

Slice Logic Utilization:

Number of Slice Registers: 11

Number of Slice LUTs: 3961

Number used as Logic: 3961

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 3968

Number with an unused Flip Flop: 3957

Number with an unused LUT: 7

Number of fully used LUT-FF pairs: 4

Number of unique control sets: 4

IO Utilization:

Number of IOs: 1547

Number of bonded IOBs: 1547

Minimum period: 13.737ns (Maximum Frequency: 72.798MHz)

Minimum input arrival time before clock: 13.278ns

Maximum output required time after clock: 26.959ns

Maximum combinational path delay: 26.501ns